

***Amendments to the Specification***

Please amend the following paragraphs/sections as indicated.

Please amend paragraph 18 as follows:

In an exemplary embodiment described below, 16-bit instructions are mapped to a 34-bit PIWF configuration that ~~support~~ supports 16-bit and 32-bit instructions. However, in alternative embodiments, the PIWF may have fewer or more than 34 bits. This environment is used for purposes of illustration. The invention, however, is not so limited. A person skilled in the art will recognize that the invention has applicability for mapping instructions (or, more generically, "data") from any first format to any PIWF configuration. Additionally, although not discussed below, each 32-bit instruction in the exemplary embodiment must also be mapped to a PIWF configuration. This may be achieved through a mapper scheme (as described below), bit stuffing, or any other mapping method known to those skilled in the art.

Please amend paragraph 30 as follows:

Multiplexor 115 receives the indicator signal from tag comparator 125, selects the desired instruction, and then transmits the desired instruction to mapper 120. Mapper 120 maps the desired instruction of the first instruction set to a PIWF configuration and transmits a mapped instruction 150 to a decoder 152. Decoder 152 decodes the mapped instructions instruction and provides control signals to execution core 155 for execution.

Please amend paragraph 35 as follows:

Instruction fetch begins as described above with respect to FIG. 1. However, the mapping and selection processes are different. Continuing with the example of the read operation, each of the data components 140 is read in parallel into a corresponding one of a plurality of mappers 211-214. For example, instruction 0 stored in data component 140A is read into corresponding mapper 211. Simultaneously, instruction 1 stored in data component 140B is read into corresponding mapper 212. Instruction 2, stored in data component 140C, is simultaneously read into corresponding mapper 213. Instruction 3 stored in data component 140D is simultaneously read into mapper 214. As further described below, an instruction is provided to mapper 215 via line 244. Thus, each instruction of a first instruction set stored in cache memory 102 is read into a corresponding one of the plurality of mappers 211-214 in parallel. Each of the plurality of mappers 211-214 maps an instruction of a first instruction set to a PIWF configuration. Each of the mapped instructions is then provided to ~~multiplexer~~ multiplexor 220 115 for selection.

Please amend paragraph 40 as follows:

Multiplexor 220 115 selects the desired instruction and transmits the selected instruction to the execution core for further processing (i.e., for instruction decoding and execution).